

Appl. No. 10/065,237  
Amdt. dated March 17, 2005  
Reply to Office action of December 17, 2004

**REMARKS/ARGUMENTS**

1. Rejection of claims 1-7 under 35 U.S.C. 103(a):

Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Moore et al. (US 6,147,863) and Shu et al. (US 6,400,843) for reasons of record that can be found on pages 2-6 in the Office action identified above.

**Response:**

The applicant would like to point out the differences between the claimed limitations of claims 1-7 and the combined teachings of Moore and Shu.

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Claim 1 contains the limitation stating that the CPU interface card comprises "a plurality of AGP contact pads interlaced with the EISA contact pads."

On the other hand, Moore does not teach the use of AGP contact pads anywhere in his disclosure. Moore does also not teach interlacing contact pads of one bus protocol with contact pads of another bus protocol on the same CPU interface card.

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Likewise Shu also does not teach interlacing contact pads of one bus protocol with contact pads of another bus protocol on the same CPU interface card. The only mention that Shu has of multiple bus protocols is in col.5, lines 45-48, where he generally says that the ISA, VESA, PCI, or AGP buses are all examples of physical buses. However, this does not teach the interlaced contact pad structure recited in claim 1.

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Therefore claim 1 is not anticipated by the combination of Moore and Shu. Claims 2-4 are dependent on claim 1, and should be allowed if claim 1 is allowed. Reconsideration of claims 1-4 is respectfully requested.

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Claim 5 contains the limitation stating that the CPU interface card comprises "a plurality of AGP contact pads disposed apart from the PCI contact pads in a predetermined distance."

5        On the other hand, neither Moore nor Shu teach this limitation. Moore teaches in Fig.1 a card 8 that is plugged into both an ISA connector 14 and a PCI connector 16. However, Shu does not teach utilizing an ISA bus as an AGP bus or utilizing an ISA connector as an AGP connector. Therefore, it would not have been obvious to combine the teachings of Moore and Shu to produce the claimed CPU interface card comprising  
10       the plurality of AGP contact pads disposed apart from the PCI contact pads at the predetermined distance.

      Claims 6-7 are dependent on claim 5, and should be allowed if claim 5 is allowed. Reconsideration of claims 5-7 is respectfully requested.

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2. Rejection of claims 8-13 under 35 U.S.C. 102(b):

      Claims 8-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Moore et al. (US 6,147,863), for reasons of record that can be found on pages 7-9 in the Office action identified above.

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**Response:**

      The applicant would like to point out the differences between the claimed limitations of claim 8 and the teachings of Moore. Claim 8 contains the limitation stating that the CPU interface card comprises "a plurality of AGP contact pads interlaced with the EISA contact pads."

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      On the other hand, Moore does not teach the use of AGP contact pads or the AGP bus anywhere in his disclosure. Moore does also not teach interlacing contact pads of one bus protocol with contact pads of another bus protocol on the same CPU interface card.

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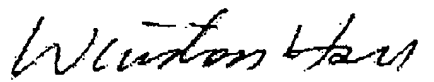
For these reasons, Moore does not anticipate claim 8, which claims the CPUT interface card with the interlaced AGP contact pads and EISA contact pads. Claims 9-13 are dependent on claim 8, and should be allowed if claim 8 is allowed. Reconsideration of claims 8-13 is respectfully requested.

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The applicant submits that claims 1-13 are patentable in view of the cited prior art, and respectfully requests that a timely Notice of Allowance be issued in this case.

Sincerely yours,

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